Docket No.: 60188-745 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Takaki YOSHIDA	:	Confirmation Number:
Serial No.:	:	Group Art Unit:
Filed: January 06, 2004	:	Examiner: Unknown

For: ERROR PORTION DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

ASSOCIATE POWER OF ATTORNEY

Mail Stop
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned Principal Attorney of record hereby appoints the following Attorneys as his Associates with regard to the above-identified application: Steven W. Allis, Reg. No. 50,532; Stephen A. Becker, Reg. No. 26,527; John G. Bisbikis, Reg. No. 37,095; Richard E. Brown, Reg. No. 47,453; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Jennifer Chen, Reg. No. 42,404; Bernard P. Codd, Reg. No. 46,429; Lawrence T. Cullen, Reg. No. 44,489; Paul Devinsky, Reg. No. 28,553; Margaret M. Duncan, Reg. No. 30,879; Shamita De. Etienne-Cummings, Reg. No. 46,072; Ramyar M. Farid, Reg. No. 46,692; Brian E. Ferguson, Reg. No. 36,801; Michael E. Fogarty, Reg. No. 36,139; John R. Fuisz, Reg. No. 37,327; Keith E. George, Reg. No. 34,111; Thomas A. Haag, Reg. No. 47,621; John A. Hankins, Reg. No. 32,029; Catherine Krupka, Reg. No. 46,227; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Michael A. Messina, Reg. No. 33,424; Dawn L. Palmer, Reg. No. 41,238; Joseph H. Paquin, Jr., Reg. No. 31,647; Scott D. Paul, Reg. No. 42,984; William D. Pegg, Reg. No. 42,988; Robert L. Price, Reg. No. 22,685; Gene Z. Rubinson, Reg. No. 33,351; Brian K. Seidleck, Reg. No. 51,321; Joy Ann G. Serauskas, Reg. No. 27,952; Jiri F. Smetana, Reg. No. 52,456; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; Michael D. Switzer, Reg. No. 39,552; David M. Tennant, Reg. No. 48,362; Judith L. Toffenetti, Reg. No. 39,048; Daniel S.

Trainor, Reg. No. 43,959; Shival P. Virmani, Reg. No. 45,032; Kelli N. Watson, Reg. No. 47,170; Cameron K. Weiffenbach, Reg. No. 44,488; Aaron Weisstuch, Reg. No. 41,557; Edward J. Wise, Reg. No. 34,523; Jeffrey A. Woller, Reg. No. 48,041; Alexander V. Yampolsky, Reg. No. 36,324; William Young, Reg. No. 54,718; Robert W. Zelnick, Reg. No. 36,976; and Wei-Chen Chen and Tomoki Tanida, admitted under 37 CFR 10.9(b) all of

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

Please continue to address all communications to the undersigned.

January 6, 2004

By _____
Michael E. Fogarty
Registration No. 36,139
Attorney for Applicant

Docket No. _____

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ERROR PORTION DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, the specification of which

(check one) X is attached hereto.

___ was filed on _____ as Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
2003-034859 (Number)	JAPAN (Country)	13/02/2003 (Day/Month/Year Filed)	X Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, D.C. 20005-3096
(202) 756-8000

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Takaki YOSHIDA

Inventor's signature Takaki YOSHIDA Date December 26, 2003
Residence* Osaka, Japan Citizenship Japan
Post Office Address 3-5-A-603, Higashiota, Ibaraki-shi, Osaka 567-0012, Japan

* City and State, or City and Country for foreign inventors